AiP74LVT16373
16bit D-type transparent latch; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2017-12-A1	2017-12	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74LVT16373 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transparent D-type latch with non-inverting 3-state bus compatible outputs.The device can be used as two 8-bit latches or one 16-bit latch. When latch enable (LE) input is HIGH, the Q outputs follow the data (D) inputs. When latch enable is taken LOW, the Q outputs are latched at the levels of the D inputs one setup time prior to the HIGH-to-LOW transition.

Features:

- 16-bit transparent latch
- 3-state buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5V bus
- Specified from -40℃ to +125℃
- Packaging information: TSSOP48

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVT16373 TA48.TB	TSSOP48	74LVT16373	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVT16373 TA48.TR	TSSOP48	74LVT16373	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

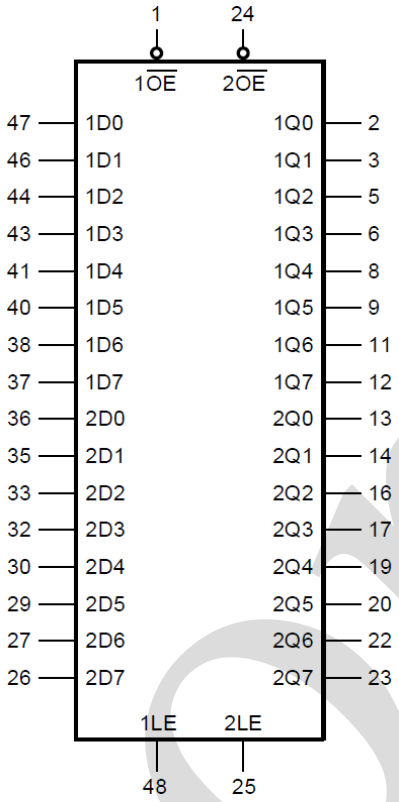


Figure 1. Logic symbol

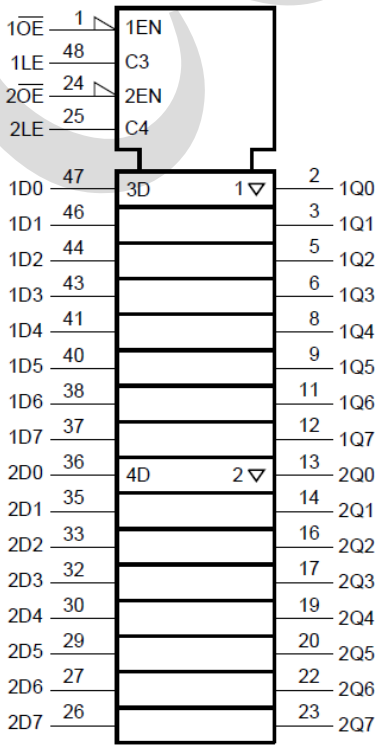


Figure 2. IEC logic symbol

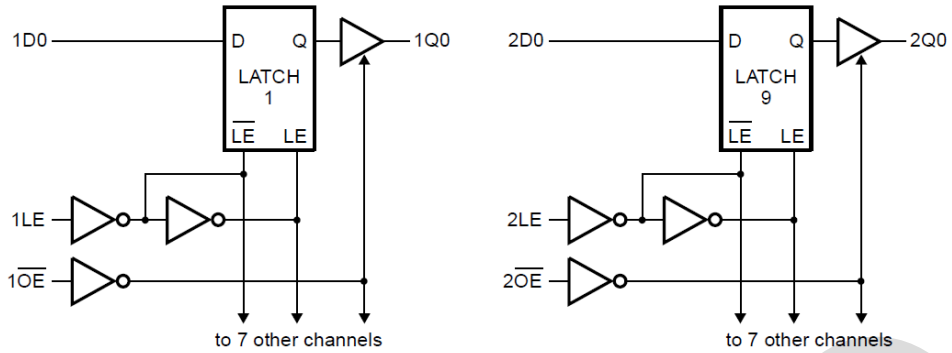
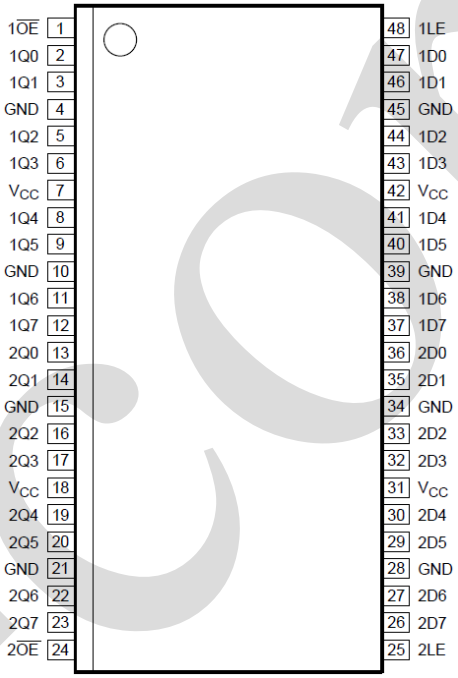


Figure 3. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
47,46,44,43,41,40,38,37	1D0,1D1,1D2,1D3,1D4,1D5,1D6,1D7	data inputs
36,35,33,32,30,29,27,26	2D0,2D1,2D2,2D3,2D4,2D5,2D6,2D7	data inputs
2,3,5,6,8,9,11,12	1Q0,1Q1,1Q2,1Q3,1Q4,1Q5,1Q6,1Q7	data outputs
13,14,16,17,19,20,22,23	2Q0,2Q1,2Q2,2Q3,2Q4,2Q5,2Q6,2Q7	data outputs
1,24	$1\overline{OE}$,$2\overline{OE}$	output enable inputs (active LOW)
48,25	1LE,2LE	Latch Enable inputs (active HIGH)
4,10,15,21,28,34,39,45	GND	ground (0V)
7,18,31,42	V_{CC}	supply voltage

2.4、Function Table

Operating mode	Inputs			Internal latches	Outputs nQn
	$n\overline{OE}$	nLE	nDn		
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	↓	l	L	L
	L	↓	h	H	H
Hold	L	L	X	NC	NC
Latch register and disable outputs	H	L	X	NC	Z
	H	H	nDn	nDn	Z

Note:

H=HIGH voltage level;

L=LOW voltage level;

↓=HIGH-to-LOW LE transition;

h=HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;

l=LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;

X=don't care;

NC=No change;

Z=high-impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+4.6	V
input voltage	V_I	-[1]	-0.5	+7.0	V
output voltage	V_O	output in OFF-state or HIGH-state[1]	-0.5	+7.0	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output current	I_O	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
junction temperature	T_j	-[2]	-	+150	℃
Soldering temperature	T_L	10s	260		℃

Note:

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.7	-	3.6	V
input voltage	V_I	-	0	-	5.5	V
input transition rise and fall rate	Δt/ΔV	outputs enabled	-	-	10	ns/V
ambient temperature	T_{amb}	in free-air	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}=-18mA		-	-0.85	-1.2	V
HIGH-level input voltage	V_{IH}	-		2.0	-	-	V
LOW-level input voltage	V_{IL}	-		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_{CC}=2.7V to 3.6V; I_{OH}=-100uA		V_{CC}-0.2	V_{CC}	-	V
		V_{CC}=2.7V; I_{OH}=-8mA		2.4	2.5	-	V
		V_{CC}=3.0V; I_{OH}=-32mA		2.0	2.3	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V; I_{OL}=100uA		-	0.07	0.2	V
		V_{CC}=2.7V; I_{OL}=24mA		-	0.3	0.5	V
		V_{CC}=3.0V; I_{OL}=16mA		-	0.25	0.4	V
		V_{CC}=3.0V; I_{OL}=32mA		-	0.3	0.5	V
		V_{CC}=3.0V; I_{OL}=64mA		-	0.4	0.55	V
HIGH-level output current	I_{OH}	-		-	-	-32	mA
LOW-level output current	I_{OL}	-		-	-	32	mA
		current duty cycle≤50%; f≥1kHz		-	-	64	mA
power-up LOW-level output voltage	$V_{OL(pu)}$	V_{CC}=3.6V; I_O=1mA; V_I=V_{CC} or GND[2]		-	0.1	0.55	V
input leakage current	I_I	all input pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
		control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
		data pins[3]	V_{CC}=3.6V; V_I=V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-	-	-5	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
bus hold LOW current	I_{BHL}	nDn input; V_{CC}=3V; V_I=0.8V		75	135	-	uA
bus hold HIGH current	I_{BHH}	nDn input; V_{CC}=3V; V_I=2.0V		-75	-135	-	uA

bus hold LOW overdrive current	I_{BHLO}	nDn input; V_{CC}=3.6V; V_I=0V to 3.6V[4]		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	nDn input; V_{CC}=3.6V; V_I=0V to 3.6V[4]		-	-	-500	uA
output high leakage current	I_{CEX}	nQn output in HIGH-state when V_O>V_{CC};V_O=5.5V; V_{CC}=3.0V		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; n$\overline{OE}$ =don't care[5]		-	-	±100	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}	V_O=3.0V	-	-	5	uA
			V_O=0.5V	-	-	-5	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=GND or V_{CC}; I_O=0A	output HIGH	-	-	0.12	mA
			output LOW	-	-	0.12	mA
			outputs disabled[6]	-	-	0.12	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V and other inputs at V_{CC} or GND[7]		-	-	0.2	mA
input capacitance	C_I	V_I=0V or 3.0V		-	3	-	pF
output capacitance	C_O	outputs disabled; V_O=0V or 3.0V		-	9	-	pF

Note:

[1] All typical values are measured at V_{CC}=3.3V and T_{amb}=25℃.

[2] For valid test results, data must not be loaded into the latches after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}=-18mA		-	-	-1.2	V
HIGH-level input voltage	V_{IH}	-		2.0	-	-	V
LOW-level input voltage	V_{IL}	-		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_{CC}=2.7V to 3.6V; I_{OH}=-100uA		V_{CC}-0.2	-	-	V
		V_{CC}=2.7V; I_{OH}=-8mA		2.4	-	-	V
		V_{CC}=3.0V; I_{OH}=-32mA		2.0	-	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V; I_{OL}=100uA		-	-	0.2	V
		V_{CC}=2.7V; I_{OL}=24mA		-	-	0.5	V
		V_{CC}=3.0V; I_{OL}=16mA		-	-	0.4	V
		V_{CC}=3.0V; I_{OL}=32mA		-	-	0.5	V
		V_{CC}=3.0V; I_{OL}=64mA		-	-	0.55	V
HIGH-level output current	I_{OH}	-		-	-	-32	mA
LOW-level output current	I_{OL}	-		-	-	32	mA
		current duty cycle≤50%; f≥1kHz		-	-	64	mA
power-up LOW-level output voltage	$V_{OL(pu)}$	V_{CC}=3.6V; I_O=1mA; V_I=V_{CC} or GND[2]		-	-	0.55	V
input leakage current	I_I	all input pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
		control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
		data pins[3]	V_{CC}=3.6V; V_I=V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-	-	-5	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
bus hold LOW current	I_{BHL}	nDn input; V_{CC}=3V; V_I=0.8V		75	-	-	uA
bus hold HIGH current	I_{BHH}	nDn input; V_{CC}=3V; V_I=2.0V		-75	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	nDn input; V_{CC}=3.6V; V_I=0V to 3.6V[4]		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	nDn input; V_{CC}=3.6V; V_I=0V to 3.6V[4]		-	-	-500	uA
output high leakage current	I_{CEX}	nQn output in HIGH-state when V_O>V_{CC};V_O=5.5V; V_{CC}=3.0V		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; $n\overline{OE}$ =don't care[5]		-	-	±100	uA
OFF-state output	I_{OZ}	V_{CC}=3.6V;	V_O=3.0V	-	-	5	uA

current		$V_I=V_{IH}$ or V_{IL}	V_O=0.5V	-	-	-5	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=GND or V_{CC}; I_O=0A	output HIGH	-	-	0.12	mA
			output LOW	-	-	0.12	mA
			outputs disabled[6]	-	-	0.12	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V and other inputs at V_{CC} or GND[7]		-	-	0.2	mA

Note:

[1] All typical values are measured at V_{CC}=3.3V and T_{amb}=25℃.

[2] For valid test results, data must not be loaded into the latches after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	nDn to nQn; see Figure 5	V_{CC}=2.7V	-	-	6.3	ns
			V_{CC}=3.0V to 3.6V	0.5	2.5	5.5	ns
HIGH to LOW propagation delay	t_{PHL}	nDn to nQn; see Figure 5	V_{CC}=2.7V	-	-	6.3	ns
			V_{CC}=3.0V to 3.6V	0.5	2.7	5.5	ns
LOW to HIGH propagation delay	t_{PLH}	nLE to nQn; see Figure 6	V_{CC}=2.7V	-	-	7.6	ns
			V_{CC}=3.0V to 3.6V	0.5	2.9	6.7	ns
HIGH to LOW propagation delay	t_{PHL}	nLE to nQn; see Figure 6	V_{CC}=2.7V	-	-	7.6	ns
			V_{CC}=3.0V to 3.6V	0.5	3.1	6.7	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	7.1	ns
			V_{CC}=3.0V to 3.6V	0.1	3.9	6.3	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	6.6	ns
			V_{CC}=3.0V to 3.6V	0.1	3.6	6.0	ns
HIGH to OFF-state propagation delay	t_{PHZ}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	7.1	ns
			V_{CC}=3.0V to 3.6V	0.1	4.6	6.3	ns
LOW to OFF-state propagation delay	t_{PLZ}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	6.6	ns
			V_{CC}=3.0V to 3.6V	0.1	4.2	6.0	ns
set-up time HIGH	$t_{su(H)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.5	0.1	-	ns
set-up time LOW	$t_{su(L)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	2.0	-	-	ns
			V_{CC}=3.0V to 3.6V	2.0	0.3	-	ns
hold time HIGH	$t_{h(H)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.0	0	-	ns

hold time LOW	$t_{h(L)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	2.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.5	0	-	ns
pulse width HIGH	t_{WH}	nLE; see Figure 6	V_{CC}=2.7V	1.5	-	-	ns
			V_{CC}=3.0V to 3.6V	1.5	0.7	-	ns

Note:

[1] Typical values are at V_{CC}=3.3V and T_{amb}=25℃.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	nDn to nQn; see Figure 5	V_{CC}=2.7V	-	-	7.6	ns
			V_{CC}=3.0V to 3.6V	-	-	6.6	ns
HIGH to LOW propagation delay	t_{PHL}	nDn to nQn; see Figure 5	V_{CC}=2.7V	-	-	7.6	ns
			V_{CC}=3.0V to 3.6V	-	-	6.6	ns
LOW to HIGH propagation delay	t_{PLH}	nLE to nQn; see Figure 6	V_{CC}=2.7V	-	-	9.1	ns
			V_{CC}=3.0V to 3.6V	-	-	8.1	ns
HIGH to LOW propagation delay	t_{PHL}	nLE to nQn; see Figure 6	V_{CC}=2.7V	-	-	9.1	ns
			V_{CC}=3.0V to 3.6V	-	-	8.1	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	8.5	ns
			V_{CC}=3.0V to 3.6V	-	-	7.6	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	7.8	ns
			V_{CC}=3.0V to 3.6V	-	-	7.3	ns
HIGH to OFF-state propagation delay	t_{PHZ}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	8.5	ns
			V_{CC}=3.0V to 3.6V	-	-	7.6	ns
LOW to OFF-state propagation delay	t_{PLZ}	n$\overline{OE}$ to nQn; see Figure 7	V_{CC}=2.7V	-	-	7.8	ns
			V_{CC}=3.0V to 3.6V	-	-	7.3	ns
set-up time HIGH	$t_{su(H)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	1.2	-	-	ns
			V_{CC}=3.0V to 3.6V	1.8	-	-	ns
set-up time LOW	$t_{su(L)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	2.4	-	-	ns
			V_{CC}=3.0V to 3.6V	2.4	-	-	ns
hold time HIGH	$t_{h(H)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	1.2	-	-	ns
			V_{CC}=3.0V to 3.6V	1.2	-	-	ns
hold time LOW	$t_{h(L)}$	nDn to nLE; see Figure 8	V_{CC}=2.7V	2.4	-	-	ns
			V_{CC}=3.0V to 3.6V	1.8	-	-	ns
pulse width HIGH	t_{WH}	nLE; see Figure 6	V_{CC}=2.7V	1.8	-	-	ns
			V_{CC}=3.0V to 3.6V	1.8	-	-	ns

Note:

[1] Typical values are at V_{CC}=3.3V and T_{amb}=25℃.

4、Testing Circuit

4.1、AC Testing Circuit

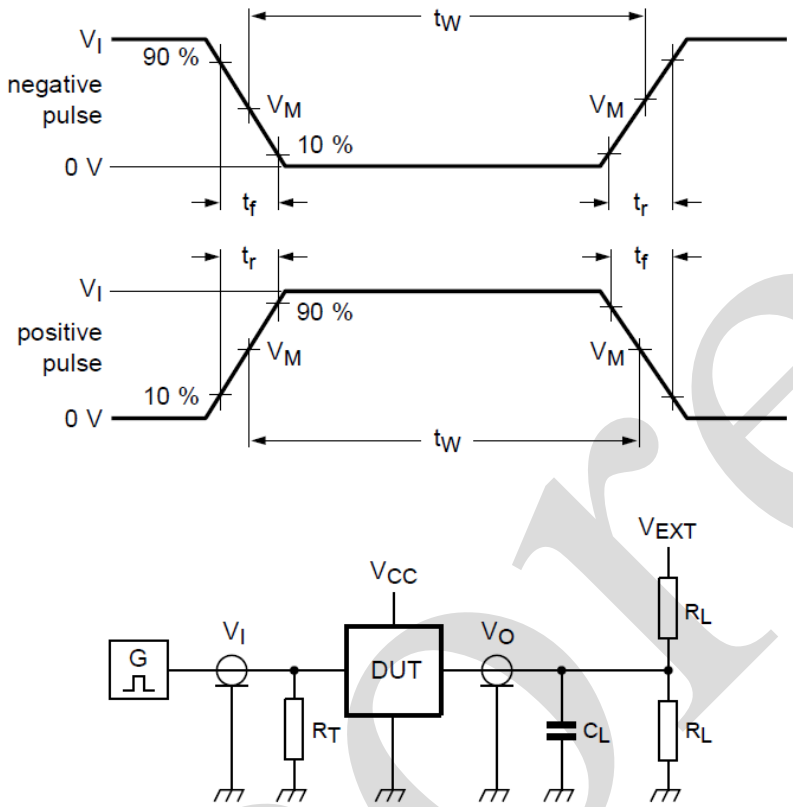


Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

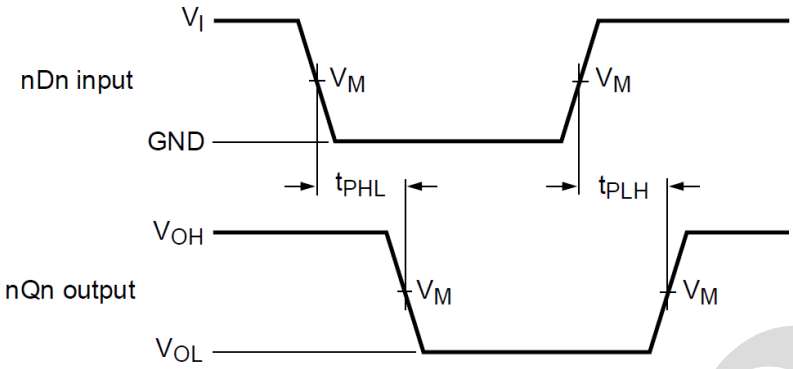
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT}=Test voltage for switching times.

4.2、Test Data

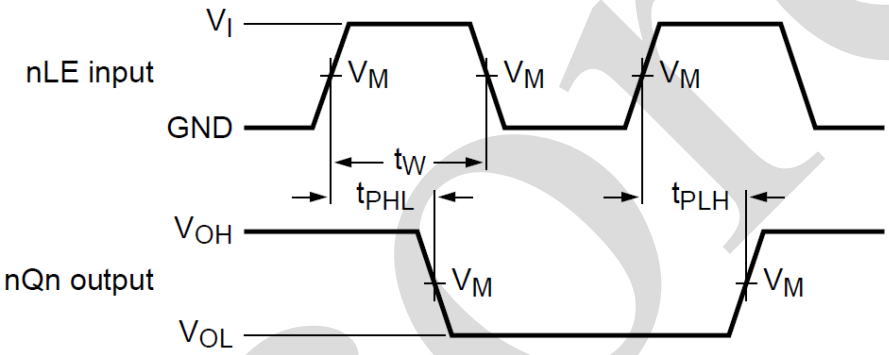
Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r , t_f	C_L	R_L	t_{PHZ} , t_{PZH}	t_{PLZ} , t_{PZL}	t_{PLH} , t_{PHL}
2.7V	≤10MHz	500ns	≤2.5ns	50pF	500Ω	GND	6V	open

4.3、AC Testing Waveforms



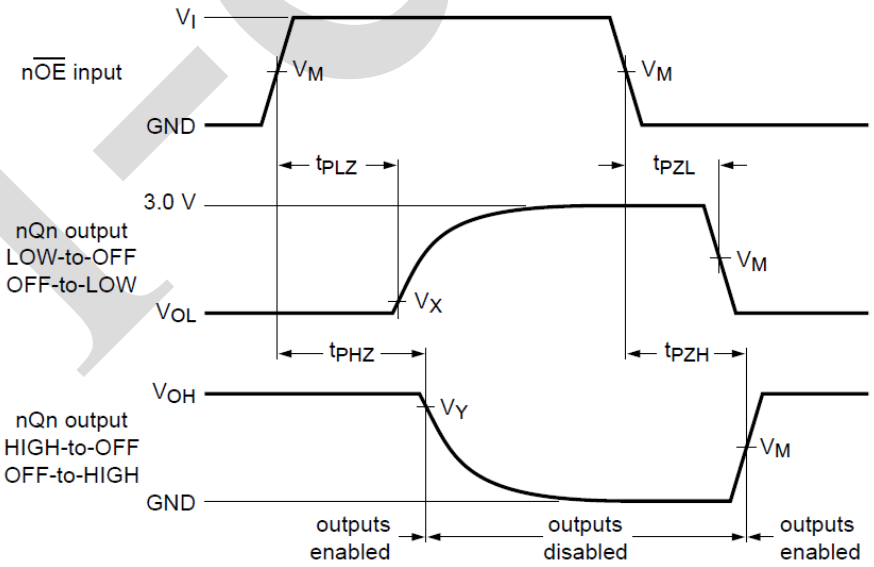
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Input (nDn) to output (nQn) propagation delays



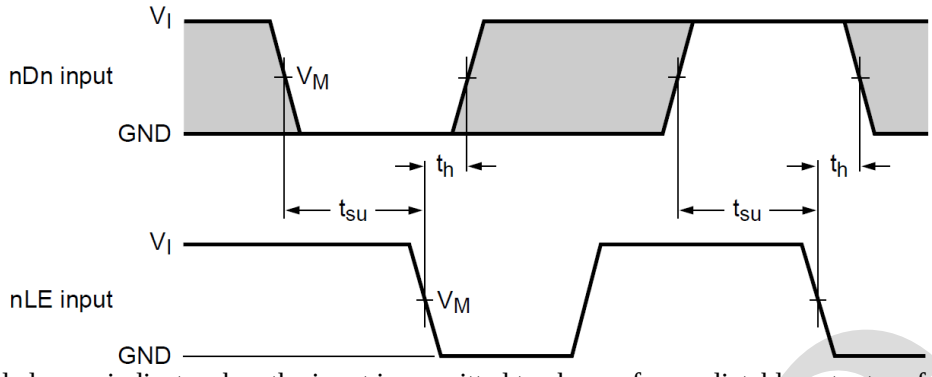
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. Latch enable input (nLE) to data output (nQn) propagation delays and pulse width



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 7. OFF-state to HIGH or LOW and HIGH or LOW to OFF-state propagation delays



The shaded areas indicate when the input is permitted to change for predictable output performance.

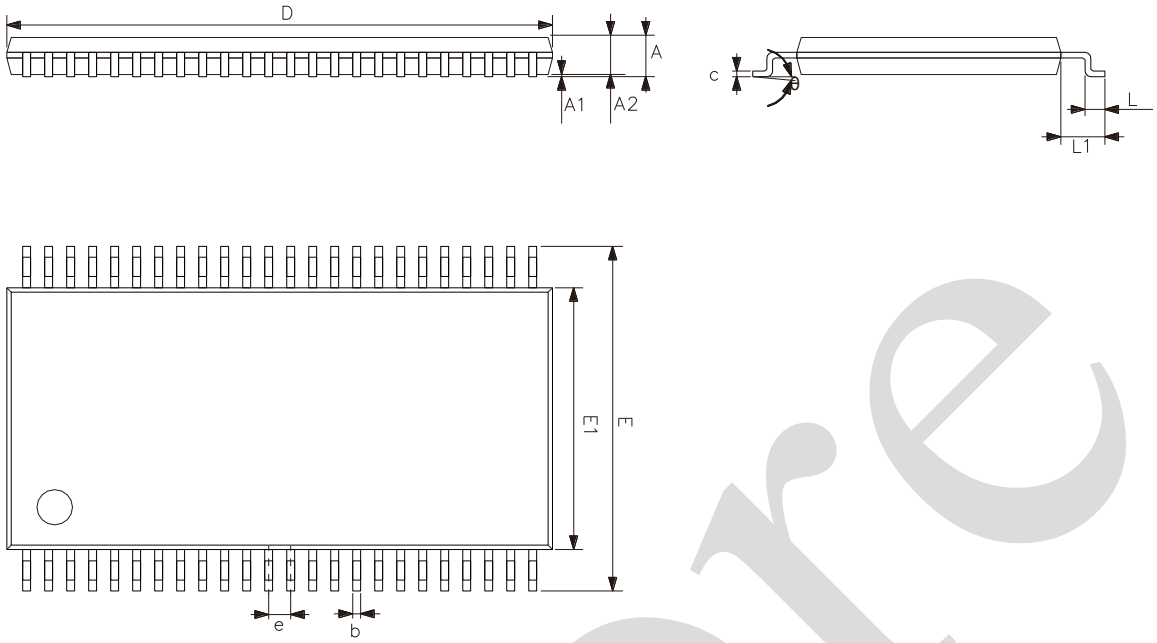
Figure 8. Input (nDn) to output (nLE) data set-up and hold times

4.4、Measurement Points

Input		Output		
V_I	V_M	V_M	V_X	V_Y
2.7V	1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V

5、Package Information

5.1、TSSOP48



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.03	0.15
A2	0.82	1.05
b	0.17	0.27
c	0.12	0.22
D	12.40	12.60
E	7.90	8.30
E1	6.00	6.20
e	0.50	
L	0.35	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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