AiP1307
Serial, I²C Real-Time Clock Chip

Product Specification

Specification Revision History:

Version	Date	Description
2023-04-A1	2023-04	New

Contents

1、General Description

AiP1307 is a low-power real-time clock (RTC). Full binary-coded decimal (BCD) clock/calendar plus 56 bytes of SRAM. Address and data are transferred serially through an 2-line bidirectional bus. The clock/calendar provides the information of seconds, minutes, hours, day, date, month, and year . The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. AiP1307 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply. Timekeeping operation continues while the part operates from the backup supply.

Features:

- Clock counting, leap year adjustment, the number of years can reach 2100 years.
- Built-in 56-byte SRAM register
- I^2C interface
- Programmable output square wave signal
- Automatic detection of power failure and power switching
- Packaging information:DIP8/SOP8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP1307SA8.TB	SOP8	AiP1307	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP1307DA8.TB	DIP8	AiP1307	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm

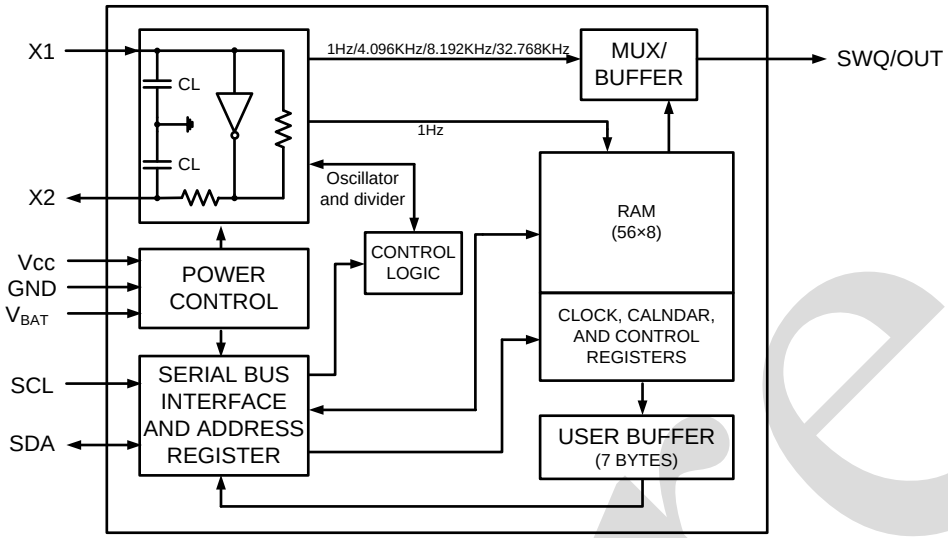
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP1307SA8.TR	SOP8	AiP1307	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing:1.27mm

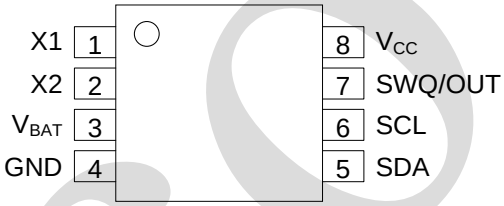
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	X1	Crystal Oscillator Input
2	X2	Crystal Oscillator Output
3	V_{BAT}	Backup Supply Input
4	GND	Ground
5	SDA	Serial Data IO
6	SCL	Serial Input Clock
7	SQW/OUT	Output fixed level when SQWE is “0”; output square wave when SQWEis “1”
8	V_{CC}	Primary Power Supply

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
input voltage	V_I	all pins except GND		-0.5 to 7.0	V
operating temperature	T_{amb}	-		-40 to +85	℃
storage temperature	T_{stg}	-		-65 to 125	℃
lead temperature	T_L	10s	DIP	250	℃
			SOP	260	℃

3.2、Recommended Operating Conditions

(T_{amb}=-40℃ to +85℃, GND=0V, unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	4.5	5.0	5.5	V
input high-level voltage	V_{IH}	2.4	-	V_{CC}+0.3	V
input low-level voltage	V_{IL}	-0.3	-	+0.8	V
backup power voltage	V_{BAT}	2.0	3.0	3.5	V

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=-40℃ to +85℃, GND=0V, V_{CC}=4.5 to 5.5V, V_{BAT}=0V, unless otherwise specified)

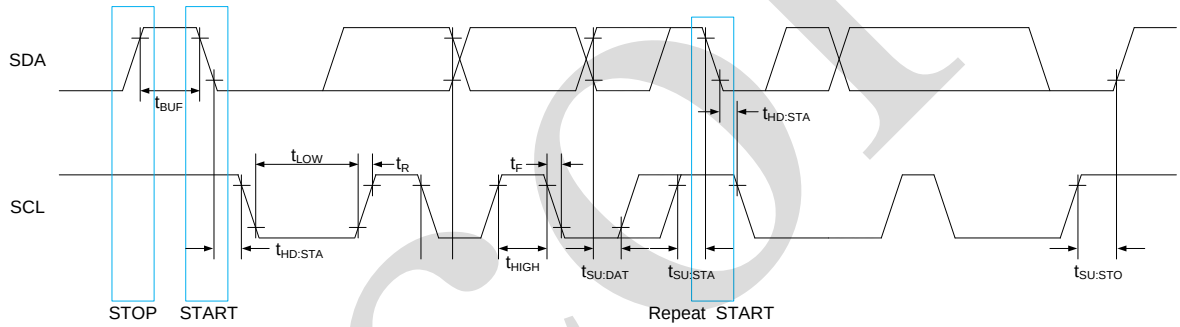
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
active supply current	I_{CCA}	V_{CC}=5V, f_{SCL}=100KHz	-	-	1.5	mA
standby curreny	I_{CCS}	V_{CC}=5V, SDA=SCL=5V	-	-	200	μA
V_{BAT} current	I_{BAT}	V_{CC}=0V, V_{BAT}=3V, SQW OUT OFF	-	300	1000	nA
		V_{CC}=0V, V_{BAT}=3V, SQW OUT ON	-	480	1000	nA
V_{BAT} data-retention current	I_{BATDR}	V_{CC}=0V, V_{BAT}=3V	-	100	-	nA
V_{BAT} leakage current	I_{BATLKG}	V_{CC}=5V, V_{BAT}=3V	-	100	-	nA
input leakage current	I_{LI}	SCL, SDA, V_{IN}=V_{CC} or GND	-1	-	1	μA
output high resistance leakage current	I_{LO}	SDA, SQW/OUT	-1	-	1	μA
output low-level voltage	V_{OL}	SQW/OUT, I_{OL}=5mA	-	-	0.4	V
power-fail voltage	V_{PF}	V_{BAT}=3V	1.216×V_{BAT}	1.25×V_{BAT}	1.284×V_{BAT}	V

3.3.2、AC Characteristics

(T_{amb}=-40℃ to +85℃, GND=0V, V_{CC}=4.5 to 5.5V, V_{BAT}=0V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	0	-	100	KHz
bus free time between a STOP and START condition	t_{BUF}	-	4.7	-	-	us
hold time (repeated) START condition	$t_{HD:STA}$	-	4.0	-	-	us
LOW period of the SCL clock	t_{LOW}	-	4.7	-	-	us
HIGH period of the SCL clock	t_{HIGH}	-	4.0	-	-	us
setup time for a repeated START condition	$t_{SU:STA}$	-	4.7	-	-	us
data hold time	$t_{HD:DAT}$	-	0	-	-	us
data setup time	$t_{SU:DAT}$	-	250	-	-	ns
rise time of both SDA and SCL signals	t_R	-	-	-	1000	ns
fall time of both SDA and SCL signals	t_F	-	-	-	300	ns
setup time for STOP condition	$t_{SU:STO}$	-	4.7	-	-	us

4、Communication Timing Diagram



5、Function Description

5.1、Detailed Description

AiP1307 is a low-power clock/calendar with 56 bytes of SRAM. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month and leap year is automatically adjusted. AiP1307 has built-in power detection circuit, which can detect power failure or automatically switch to standby power supply.When V_{CC} falls below 1.25×V_{BAT}, the device terminates and resets the device address counter to prevent erroneous data from being written to the device. When V_{CC} falls below V_{BAT}, the device switches into a battery-backup mode. The device switches from battery to V_{CC} when V_{CC} is greater than V_{BAT}+0.2V and the communication is valid when V_{CC} is greater than 1.25×V_{BAT}.

5.2、Oscillator Circuit

Characteristic	Symbol	Min.	Typ.	Max.	Unit
nominal frequency	f_o	-	32.768	-	KHz
serial resistance	ESR	-	-	45	KΩ
load capacitance	C_L	-	12.5	-	pF

5.3、Register Description

The following table shows the address map for the AiP1307 RTC and SRAM registers. The RTC registers are located in address locations 00H to 07H. The SRAM registers are located in address locations 08H to 3FH. During a multibyte access, when the address pointer reaches 3FH, it will automatically jump to 00H.

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BT1	BIT0	Function	Range
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12	PM/AM	10 Hour	Hours				hours	1-12+AM/PM
		24	10 Hour							0-23
03H	0	0	0	0	0	Day			Day	01-07
04H	0	0	10 Date		Date				Date	01-31
05H	0	0	0	10 Month	Month				Month	01-12
06H	10 Year				Year				Year	00-99
07H	OUT	0	0	SQWE	0	0	RS1	RS0	Control	-
08H-3FH	-								RAM 56×8	00H-FFH

Note: When power on, the status of RTC and RAM registers is uncertain, and initialization configuration is required.

5.4、Clock And Calendar

The time and calendar information is obtained by reading the appropriate register bytes. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. The day-of-week register increments at midnight. The clock register adopts BCD format, BIT 7 of second register is the clock halt (CH) bit. When CH=1, the oscillator is disabled. When CH=0, the oscillator is enabled. When power-on, CH needs to be set to “0” because the state of the register is undefined.

Bit 6 of the hour register is defined as the 12-hour or 24-hour mode selection bit. When BIT6=1, the 12-hour mode is selected. In the 12-hour mode, BIT5 is the AM/PM bit and the logic high is PM when BIT5=1. In the 24-hour mode, the fifth bit is the second 10-hour bit (20 to 23 hours). The hours value must be re-entered when the 12/24-hour mode bit is changed.

The week register is incremented at midnight, and the value of the week is defined by the user(i.e., if 1 equals Sunday, then 2 equals Monday, and so on).

5.5、Control Register

AiP1307 control register is used to control the operation of SQW/OUT pin.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OUT	0	0	SQWE	0	0	RS1	RS0

Bit7: Output Control (OUT). When SQWE=0, BIT7 controls the output level state of SQW/OUT.

Bit4: Square-Wave Enable (SQWE). When SQWE=1, SQW/OUT outputs a square wave. The output frequency is selected by RS1 and RS0.

Bits 1 and 0: Rate Select (RS1, RS0**).** When the square wave output is enabled, these two bits control the square wave frequency of the output.

The truth table of the control register is as follows:

SQWE	OUT	RS1	RS0	SQW/OUT Output
0	0	X	X	0
0	1	X	X	0
1	X	0	0	1Hz
1	X	0	1	4.096KHz
1	X	1	0	8.192KHz
1	X	1	1	32.768KHz

5.6、Introduction of Communication Mode

The AiP1307 supports the I^2C protocol. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The AiP1307 operates as a slave on the I^2C bus.

The following points shall be paid attention to during I^2C communication: 1. Data transfer can be initiated only when the bus is not busy. 2. During data transfer, the data line must remain stable as long as the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals. Accordingly, the following bus conditions have been defined:

A. Bus not busy: Both data and clock lines remain HIGH.

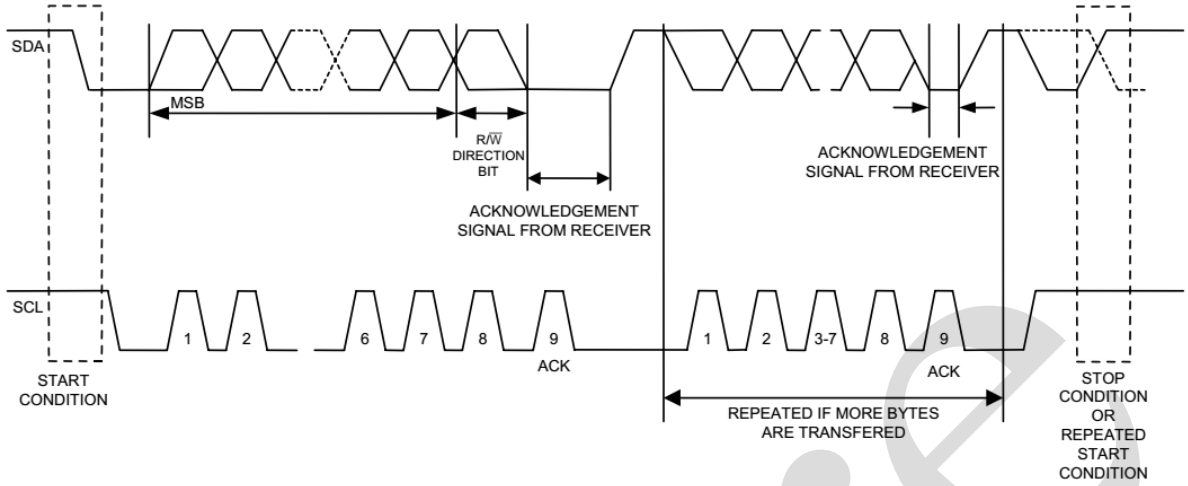
B. START data transfer: The data line changes from HIGH to LOW when the clock line is HIGH.

C. STOP data transfer: The data line changes from LOW to HIGH, when the clock line is HIGH.

D. Data valid: After a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. AiP1307 operates in the standard mode (100kHz) only.

E. Acknowledge: When Each receiving device is addressed, it is obliged to generate an acknowledge after thereception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse and the SDA line keeps LOW during the HIGH period of the clock pulse. A master signal issues an end signal to the slave by not generating an acknowledgement on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.



The above figure details how data is transferred on the I^2C bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

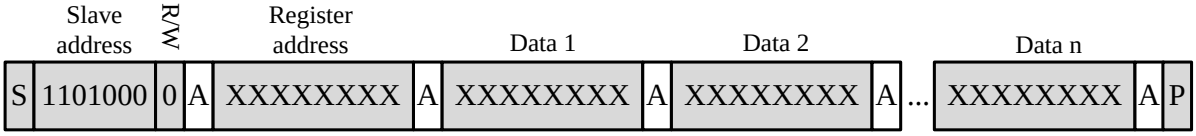
(1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

(2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The AiP1307 can operate in the following two modes:

(1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL.After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AiP1307 address, which is 1101000, followed by the direction bit (R/W). After the AiP1307 acknowledges the slave address + write bit, the master transmits a one-byte address to the AiP1307. This sets the register pointer on the AiP1307, then AiP1307 acknowledges the transfer. The master can then transmit zero or more bytes of data, then AiP1307 acknowledges each byte received. The register pointer automatically increments after each data byte are written. The master will generate a STOP condition to terminate the data write.

Communication timing sequence of Write Mode：



S:Start

A:Acknowledge(ACK)

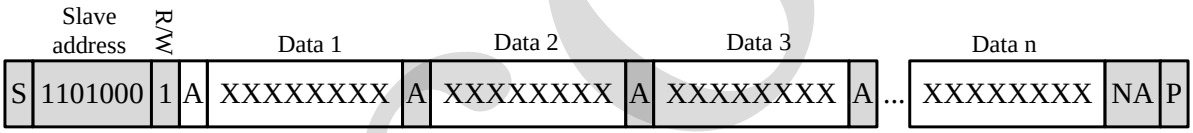
P:Stop

Master to slave

Slave to master

(2) **Slave Transmitter Mode (Read Mode):** AiP1307 transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit AiP1307 address(1101000) and the direction bit (R/W), which is read for 1. Then AiP1307 outputs an acknowledge on SDA. Afterwards, AiP1307 begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The register pointer automatically increments after each byte are read. The AiP1307 must receive a Not Acknowledge to end a read.

Communication timing sequence of Data Read Mode:



S:Start

A:Acknowledge(ACK)

NA:Not acknowledge

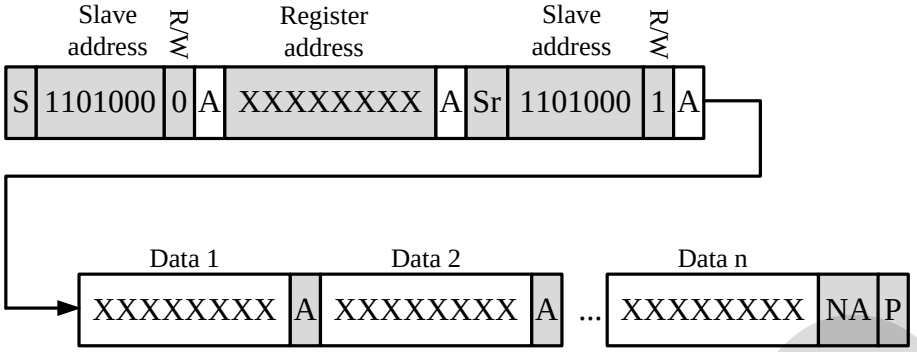
P:Stop

Master to slave

Slave to master

After reading the last byte of data, the master gives a non-acknowledgement signal (pulling the SDA bus high) to notify the AiP1307 that the read operation is complete.

Data Read (Write Pointer, Then Read)—Slave Receive and Transmit

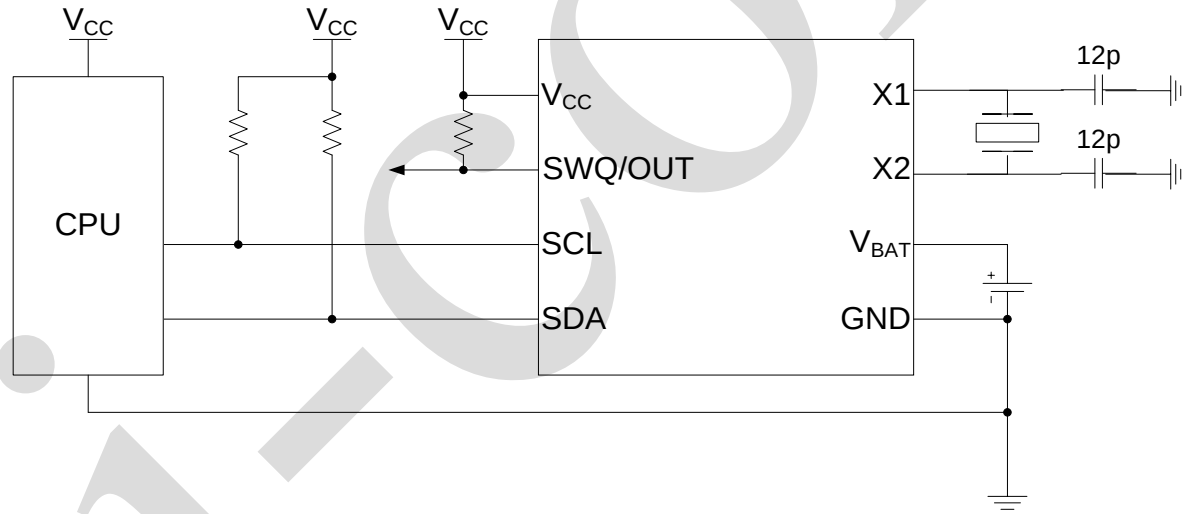


S:Start Sr:Repeated Start Master to slave

NA:Not acknowledge

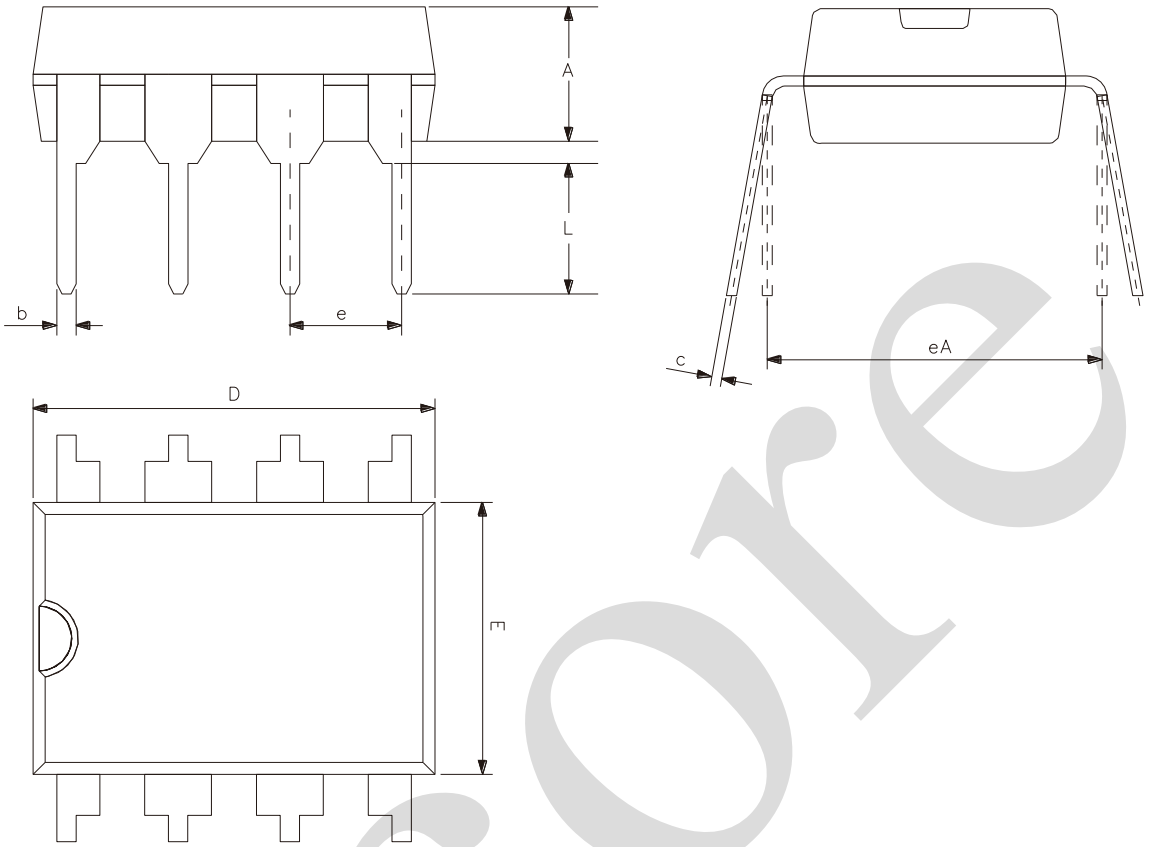
A:Acknowledge(ACK) P:Stop Slave to master

6、Typical Application Circuit



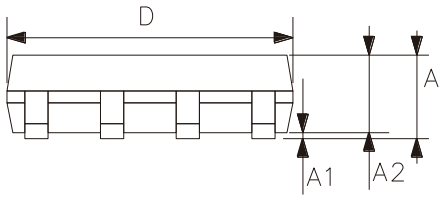
7、Package Information

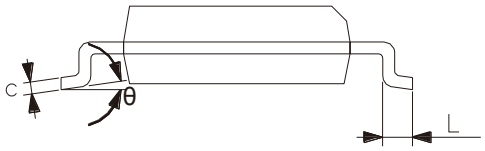
7.1、DIP8

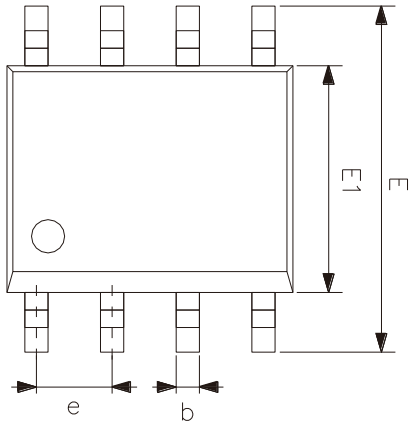


Symbol	Dimensions (mm)	
	Min.	Max.
A	3.00	3.60
b	0.36	0.56
c	0.20	0.36
D	9.00	9.45
E	6.15	6.60
e	2.54	
eA	7.62	9.30
L	3.00	-

7.2、SOP8







Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.05	0.25
A2	1.25	1.55
D	4.70	5.10
E	5.80	6.30
E1	3.70	4.10
b	0.306	0.51
c	0.19	0.25
e	1.27	
L	0.40	0.89
θ	0 °	8 °

8、Statements And Notes

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

8.2、Notes

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